performing an etching step to remove a portion of the gap fill polymer layer remaining on the inside of the via hole, forming a partial gap fill polymer, while the dielectric layer is substantially not etched in this etching step;

performing a lithographic process to form a photoresist layer having an opening above the dielectric layer, wherein the opening exposes the via hole and the partial gap fill polymer;

etching a portion of the dielectric layer exposed in the opening, to form a trench in the dielectric layer;

removing the photoresist layer and the partial gap fill polymer, to expose a portion of the conductive layer; and

filling the via hole and the trench with a metal material, to simultaneously form a plug and a first conductive line.

2. The method of claim 1, wherein forming at least one via hole includes forming a plurality of isolated via holes and a plurality of dense via holes, wherein a distance between neighboring dense via holes is smaller than a distance between neighboring isolated via holes.

3. The method of claim 1, wherein the etching step for removing a portion of the gap fill polymer layer remaining on the inside of the via hole includes anisotropic etching.

4. The method of claim 1, wherein the conductive layer in the substrate includes a second conductive line.

5. The method of claim 1, wherein a material of the dielectric layer includes silicon oxide.

7. A dual damascene partial gap fill polymer fabrication process, comprising:

providing a substrate having a conductive layer therein, and a passivation layer formed over the conductive layer;

sequentially forming a first dielectric layer, a first etching stop layer and a second dielectric layer over the passivation layer;

sequentially patterning the second dielectric layer, the etching stop layer and the first dielectric layer to form at least one via hole, which exposes a portion of the passivation layer;

covering the second dielectric layer with a gap fill polymer layer, to fill the via hole;

performing a chemical mechanical polishing step to remove gap fill polymer layer on the

outside of the via hole;

performing an etching step to remove a portion of the gap fill polymer layer remaining in the via hole, in order to form a partial gap fill polymer, while the second dielectric layer is substantially not etched in this etching step;

performing a lithographic process to form a photoresist layer having an opening above the second dielectric layer, wherein the opening exposes the via hole and the partial gap fill polymer;

etching the exposed second dielectric layer until the etching stop layer is reached, to form a trench in the second dielectric layer;

removing the photoresist layer and the partial gap fill polymer;

removing the passivation layer on a bottom of the via hole to expose a portion of the conductive layer; and

filling the trench with a metal material to simultaneously form a plug and a first conductive line.

8. The method of claim 7, wherein forming at least one via hole includes forming a plurality of isolated via holes and a plurality of dense via holes, wherein a distance between neighboring dense via holes is smaller than a distance between neighboring isolated via holes.

9. The method of claim 7, wherein the etching step for removing a portion of the gap fill polymer layer remaining in the via hole includes anisotropic etching.

10. The method of claim 7, wherein the conductive layer in the substrate includes a second conductive line.